AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) An apparatus for estimating power consumption, comprising:

a behavioral synthesis unit to which an algorithm-level description is input for converting the algorithm-level description to a clock-based description and behavioral synthesis information; and

a clock-based simulation unit to which the clock-based description and behavioral synthesis information are input for executing a clock-based simulation and calculating a power consumption factor ~~of a storage element based upon both the clock-based description and behavioral synthesis information~~ by tracing a state of a variable in the clock-based description, wherein the power consumption factor of ~~the~~ a storage element is calculated by determining whether an array variable in the clock-based description is mapped to a memory or to registers, using the behavioral synthesis information.

2. (Canceled)

3. (Currently amended) The apparatus according to claim 1, wherein the power consumption factor for said storage element comprises at least one of toggle rate and transition probability.

4. (Canceled)

5. (Previously presented) The apparatus according to claim 1, wherein a correspondence between RT (register transfer) variable names and gates is assumed from the behavioral synthesis information, and the at least one of toggle rates and transition probabilities are set in gate circuits, thereafter the at least one of toggle rates and transition probabilities of all gate circuits being calculated.

6. (Currently amended) The apparatus according to claim 3, wherein if a gated clock is provided, the at least one of toggle rate and transition probability of a clock are made the same as ~~the~~ a write probability with respect to a storage element.

7. (Currently amended) A method of estimating power consumption, comprising :

inputting a clock-based description and behavioral synthesis information;

executing a clock-based simulation based upon the clock-based description; and

calculating a power consumption factor by tracing a state of a variable in the clock-based description, ~~based upon both the clock-based description and behavioral synthesis information,~~ wherein the power consumption factor of ~~the~~ a storage element is calculated by determining whether an array variable in the clock-based description is mapped to a memory or registers, using the behavioral synthesis information.

8. (Canceled)

9. (Currently amended) The method according to claim 7, wherein the power consumption factor of said storage element comprises at least one of toggle rate and transition probability.

10. (Canceled)

11. (Previously presented) The method according to claim 9, further comprising :

assuming a correspondence between RT (register transfer) variable names and gates from the behavioral synthesis information;

setting the at least one of toggle rates and transition probabilities in gate circuits; and~~,~~

thereafter, calculating the toggle rates and transition probabilities of all gate circuits.

12. (Currently amended) The method according to claim 9, wherein, if a gated clock is provided, the at least one of toggle rate and transition probability of a clock is made the same as ~~the~~ a write probability with respect to the storage element.

13. (Currently amended) A method of simulation of a device, said method comprising:

providing, into a clock-based simulation module, a clock-based description and behavioral synthesis information, said behavioral synthesis information including information for describing which of alternative types of storage units has been simulated;

executing a clock-based simulation in said clock-based simulation module; and

calculating a power consumption as based on first executing a clock-based simulation using a format wherein each bit in a storage element is separately identifiable and then using information from the behavioral synthesis to finalize a power estimation for the storage element for said storage element, to be appropriately based upon knowing a specific architecture of said storage element.

14. (Previously presented) The method of claim 13, further comprising:

calculating a power consumption factor for each bit in said storage element, during the clock-based description and determining from the behavioral synthesis information a type of storage unit that will be used for said storage element.

15. (Previously presented) The method of claim 13, wherein said clock-based description is received as an output from a behavioral synthesizing unit, based upon an algorithm description received by said behavioral synthesizing unit.

16. (Previously presented) The method of claim 13, wherein said information on storage unit type is received as an output from a behavioral synthesizing unit, based upon an algorithm description received by said behavioral synthesizing unit.

17. (Previously presented) The method according to claim 14, wherein the power consumption factor comprises at least one of a toggle rate and a transition probability.

18. (Previously presented) The method according to claim 13, further comprising:

assuming a correspondence between RT (register transfer) variable names and gates from the behavioral synthesis information;

setting at least one of toggle rates and transition probabilities in gate circuits; and

calculating toggle rates and transition probabilities of all gate circuits.

19. (Currently amended) The method according to claim 18, wherein, if a gated clock is provided, the at least one of toggle rate and transition probability of a clock are made the same as ~~the~~ a write probability with respect to a storage element.

20. (Previously presented) The apparatus according to claim 1, wherein the clock-based simulation unit calculates the power consumption factor of the storage element by tracking transitions of each index bit of an array variable during the clock-based simulation when the array variable is mapped to the registers.